LTspice Modeling for GaN-GIT HEMT Including Cryogenic Temperature

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Abstract. Highly efficient electrically driven avionics have led to a renewed interest in cryogenic propulsion systems with the goal of reducing carbon emission footprint. Although cryogenic converters promise better efficiency and improved power density, the successful design is incumbent upon the appropriate switching device selection and simulation-based analyses prior to initial prototyping. In this work, a datasheet-driven compact model for a gallium nitride (GaN) Gate Injection Transistor (GIT) has been proposed and implemented in LTspice, a versatile, high performance, and free circuit simulator in order to investigate the merit of the chosen device in a power electronic system.

1. Introduction

Power electronics is now the key enabler to reducing aircraft mass, fuel consumption, and CO2 footprint as the aviation industry is committed to modernizing the energy system of aircraft and introducing more electric aircraft (MEA) and fully electric aircraft (FEA). The power system for large aircraft requires a high-power density. A transition toward cryogen-cooled and fueled fully electric aircraft is proposed in order to lower the weight and size of power system components, even though the historically cryogenic operation was mostly focused on spacecraft-based electronic applications [1]. Compared to their ambient counterpart, the cryogenic performance of power electronic converters offers a more ambitious solution. Since superconducting coils offer substantially higher current densities and flux densities, which decrease the use of iron materials, superconducting motors and generators are becoming more and more relevant. To prevent unnecessary thermal insulation and temperature control systems and to increase power density, the power electronic converters must be integrated with the superconducting electric machine [2]. Designers must select appropriate semiconductor devices for each switching position in order to create a converter with greater efficiency and increased power density. Due to their starkly different characteristics, switching semiconductor devices at cryogenic temperatures has remained a problem for designers [3]. the successful design is incumbent upon the appropriate switching device selection and simulation-based analyses prior to initial prototyping.

A commercial GaN GIT (31A/600V) has been characterized for this work. Although existing literatures [4-7] proposed compact modeling of GaN GITs [8-10], none of them extend to cryogenic temperatures. Moreover, the available models do not take the hole injection related phenomenon into account. The vendor's provided model [10] lacks the non-linearity in capacitance modeling which arises from the field-plates. In this work, a datasheet-driven compact model for a gallium nitride (GaN) Gate Injection Transistor (GIT) with cryo-compatible temperature scaling equations has been proposed and

implemented in LTspice, a flexible, high-performance, and free circuit simulator. In addition, a 5-level cascaded H-Bridge inverter has been simulated to demonstrate the convergence properties of the model.

2. Device Operation Principle

A very desirable attribute for safe operation in power electronics is the support of a usually off operation. The gate injection transition (GIT), a very promising gate structure enables this by allowing the depletion of the two-dimensional electron gas (2DEG) under the gate terminal at zero bias. With the exception of the fact that it exhibits "conductivity modulation" at higher gate voltages, the structure is quite similar to that of a JFET. By injecting holes at the interface along with the (2DEG), this characteristic makes it possible to have a lower on-state resistance [11].

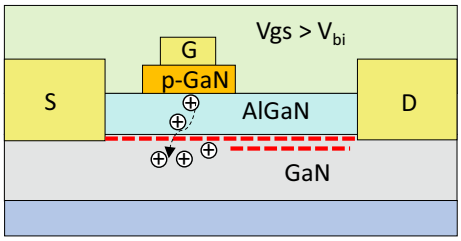

Figure 1. Cross section of a GaN GIT device structure.

Figure 1 illustrates the cross-sectional view and operation principle of a GaN GIT. As illustrated, the GIT consists of a pGaN underneath the typical gate material. Not only does the gate modulate the 2DEG concentration, but it also allows for hole injection which leads to a reduced on-resistance. Since the 2DEG is fully depleted at V_{gs}=0 V, E-mode operation can be ensured. Figure 2(a) demonstrates the off-state band diagram. It is apparent that the Fermi energy level is well below the conduction band which prohibits 2DEG accumulation in the quantum well.

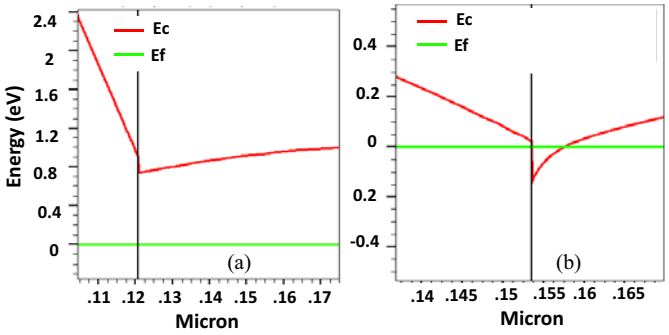

Figure 2. (a) Off-state band diagram when $V_{gs} < V_{th}$ (b) On-state band diagram when $V_{th} < V_{gs} < V_{bi}$.

Increasing V_{gs} to the point where $V_{th} < V_{gs} < V_{bi}$, where V_{bi} is the built-in potential of the p-n junction, results in the 2DEG modulation that is typical of unipolar FET devices. Figure 2(b) demonstrates the band diagram at on-state. As can be seen from the figure, the fermi level inside the quantum well allows for abundant 2DEG. Hole injection into the 2DEG channel originates from p-GaN whenever the V_{gs} exceeds the V_{bi}.

3. Model Development

The available subcircuit based compact models using primitive SPICE elements are inadequate to model the p-n junction-based GaN GIT HEMT gate. Available compact models either use of empirical current definition or considers full-fledged analytical calculation which necessitates iterative solution resulting in an extended simulation time. In addition, none of the previous models [8-10] considers the second source of current conduction once the gate voltage reaches beyond the junction built-in voltage.

Furthermore, the temperature scaling is only limited to room temperature and higher [11] which, if extrapolated, will result inadvertently wrong results. One interesting phenomenon that can be observed from the transconductance curve is the presence of two humps unlike typical FETs, which is due to the hole injection during conductivity modulation. Unlike its silicon counterparts, GaN HEMT 2DEG does not show any "carrier-freezeout" effect and therefore a perfect candidate for cryogenic power electronics [15]. Finally, the available GaN-GIT models [8, 10] do not incorporate the multiple non-linear humps owing to the depletion associated with multiple field-plates. The proposed model uses a phenomenological modeling of the intrinsic capacitances. Vendor's provided model uses conventional JFET based SPICE capacitance modeling [10] which fails to incorporate the transition in capacitance at filed-plate pinch-off voltage. The model is implemented in LTspice which is a freely available popular power electronics circuit simulator.

3.1. First Quadrant Characteristics

The first quadrant operation is described with the following equations:

$$I_{dsLIN} = \frac{Z_g K_p}{d_{AlGaN} L_g}\left[(V_{gs} - V_{th})V_{ds} - \frac{1}{2}V_{ds}^2\right] \tag{1}$$

$$I_{dsSAT} = \frac{Z_g K_p (V_{gs} - V_t - V_{dssat}) E_c}{d_{AlGaN}} \tag{2}$$

Equation (1) describes the linear region operation while Equation (2) describes the saturation region operation. Here, Z_g is the width, L_g is the channel length, d_{AlGaN} is the AlGaN barrier layer thickness, K_p is the transconductance parameter. V_{ds}, V_{gs} and V_{dssat} are the drain-source voltage, gate-source voltage, and drain-source saturation voltage respectively.

3.2. Third Quadrant Characteristics

transconductance parameter. V_{ds}, V_{gs} and V_{dssat} are the drain-source voltage, gate-source voltage, and drain-source saturation voltage respectively. It should be noted that velocity saturation has been incorporated to formulate the saturation since it actively contributes to small channel and

The third quadrant operation is described with the following equations:

$$I_{ds3LIN} = -\frac{Z_g K_{p3}}{d_{AlGaN} L_g}\left[(V_{gd} - V_{th3})V_{sd} - \frac{1}{2}V_{sd}^2\right] \tag{3}$$

$$I_{ds3SAT} = \frac{Z_g K_{p3} (V_{gd} - V_{th3} - V_{sdsat3}) E_c}{d_{AlGaN}} \tag{4}$$

Please note that the polarity of the voltages and current has been adjusted. Furthermore, the transconductance parameter and threshold voltage is independent of the first quadrant characteristics dur to the inherent asymmetry of the device structure [16].

3.3. Gate-Drain Drift Resistance

To withstand the high off-state voltage, the gate-drain length is intentionally kept larger than the gate-source length. The drain access resistance is highly non-linear in nature and is expressed as the following equation [11]:

$$R_{dr} = \frac{R_{del1}}{1 + \gamma V_{gs}} \ln\left(1 + \exp\left[\left(b_0 + b_1 V_{gs}\right) V_{ds} - d_0 - d_1 V_{gs} - d_2 {V_{gs}}^2\right]\right) \quad (5)$$

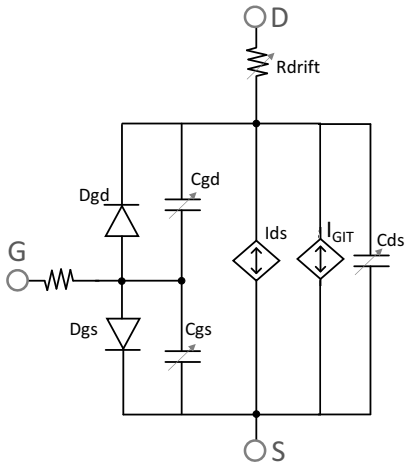

Figure 3. Equivalent circuit representation of GaN GIT.

Figure 3 illustrates the equivalent circuit representation of the GIT. Please note that there is a parallel branch to model the hole current after the V_{gs} exceeds V_{bi}.

3.4. Conductivity Modulation Modeling

As discussed above, the Id-Vgs curve of a GIT-GaN HEMT demonstrates a 2nd peak at higher gate voltage which is a sign of 'conductivity modulation' as shown in Figure 5(b). In this work, a secondary path for channel current has been defined as the gate voltage surpasses the built-in potential. The formulation is given by equation 6. The current being due to the holes, the mobility term and transconductance parameter have been separately defined from the electron current.

$$I_{dsGIT} = \mu_h K_h \left(v_{gsGIT}\right)^{VGEXP} \tanh\left[\alpha V_{ddsp}\right] \left(1 + \lambda V_{ddsp}\right) \quad (6)$$

Here VgsGIT is defined as Vgs-Vbi. The tanh(x) dictates the smooth transition between linear and saturation regime as described in [17]. The parameters α and VGEXP determines the smooth transition between these two regions.

3.5. Non-Linear Interelectrode Capacitance

Due to the presence of field-plates, the depletion of 2DEG takes place at different pinch-off voltages which causes non-linearity in C-V behaviour of the GaN HEMT as demonstrated in Figure 4.

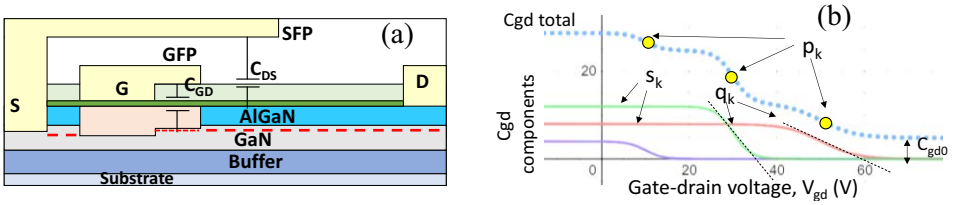

Figure 4. (a) Field plate induced depletion causes non-linearity inter-electrode capacitance behavior, (b) important parameter extraction regions of a Cgd-Vgd curve.

The C-V characteristics has been expressed as the following equation [11]:

$$C_{gdk} = \sum_{k=1}^{n} \frac{s_{gdk}}{1 + exp\left(\frac{p_{gdk} - v_{gd}}{q_{gdk}}\right)} + C_{gd0} \tag{7}$$

Here each term controls a specific region of the C-V characteristics as illustrated in Figure .4(b) The number *n* depends on the number of field plates connected at different terminals.

4. Model Validation

The developed model is implemented in the LTspice platform. The overlaid simulated results and the experimental/datasheet values are given in this Section. In this section, the device data in [12] is used as an example to validate the accuracy of the proposed model. Figure 5(a) presents the Id-Vgs characteristics and Figure 5(b) shows gm-Vgs plot with both simulated and measured data overlaid. As evident from the figures, the model can fit the slope change around Vgs = 4V, which is even clearer from the gm-Vgs plot demonstrating a second peak. The comparisons of the 1st quadrant Id-Vds characteristics between the simulated results and datasheet values are presented in Figure 5(c). The model can accurately describe the voltage-dependence of the device capacitances thanks to its flexible nature for filed plate variation. Figure 5(d) shows the 3rd quadrant Id-Vds characteristics between the model results and datasheet values. The modeling results show good agreement with the datasheet. Figure 5(e) presents the comparison of the simulated vs. datasheet value for parasitic capacitance as a function of Vds.

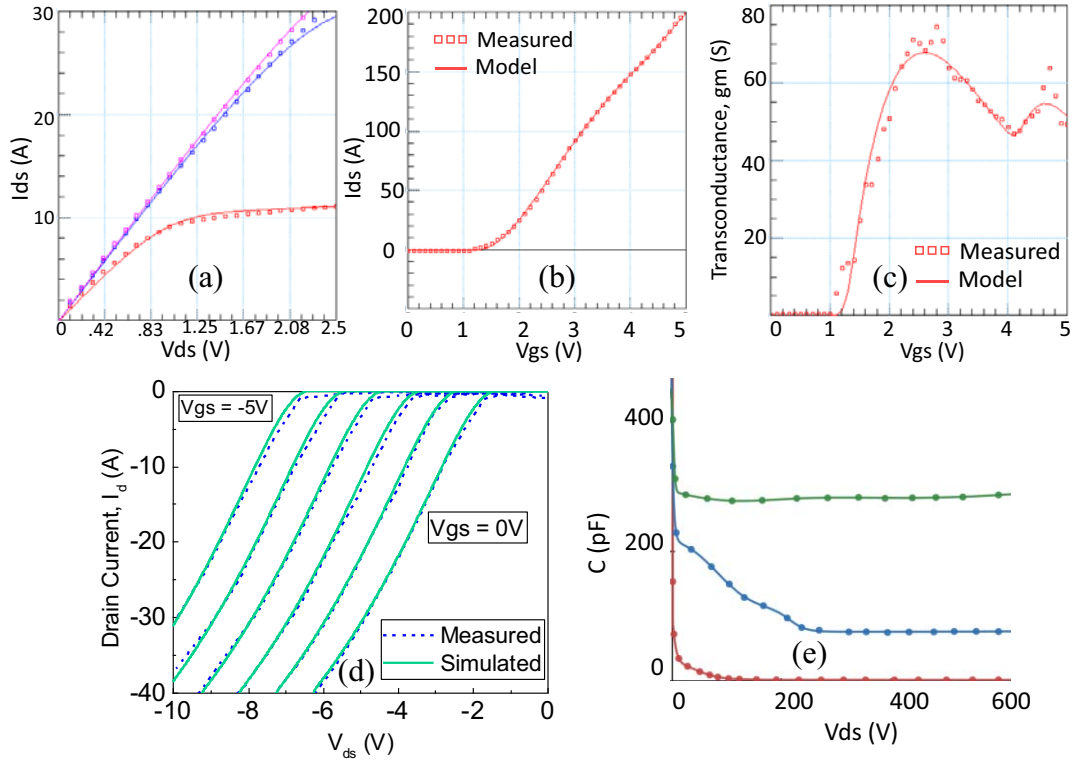

Figure 5. Nonlinearity in transfer curve in a GIT due to hole injection [12], (b) Second gm peak due to hole injection [12], (c) Id-Vds characteristics at 25°C (Vgs=2-4 V), (d) Third quadrant characteristics overlaid with the datasheet values (e) C-V characteristics as a function of Vds.

5. Cryogenic Test Setup

5.1. Test Setup

The device is characterized at cryogenic temperature with LN_2. A PCB was designed to characterize multiple devices simultaneously [14] to effectively use the resources. The test setup is demonstrated in Figure 6(a). The 4-wire Kelvin connection was used to de-embed the long cable induced resistance as illustrated in Figure 6(b) and 6(c). The PCB was kept inside a delta design thermal chamber with a custom front panel with BNC connectors. The LN_2 was injected into the chamber by a flexible metal transfer line through a solenoid valve. The temperature can be set from the front panel. Sufficient time has been provided for the temperature to reach a steady-state value. Keysight B1505A parametric analyzer has been used for I-V and C-V characterization. Pulsed measurements have been undertaken to avoid/minimize self-heating of the device under test (DUT).

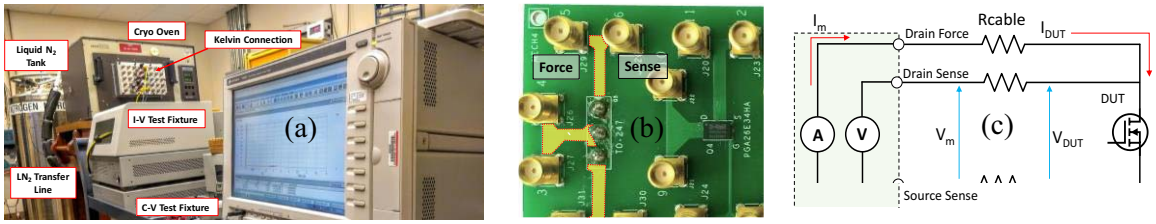

Figure 6. (a) Cryogenic experimental setup, (b) PCB for multiple device testing at cryogenic temperature with Kelvin connections (4-wire measurement), (c) Kelvin principle [3].

5.2. Test Results

Figure 7 depicts a commercial (PGA26E07BA) GIT's property at ambient temperature and cryogenic temperatures. The on resistance reduces due to an increase in electron mobility. The increase in the threshold voltage can be attributed to the hole injection from the metal gate to the p-GaN layer and their accumulation near the interface. The transconductance increases with the channel mobility and carrier velocity increase.

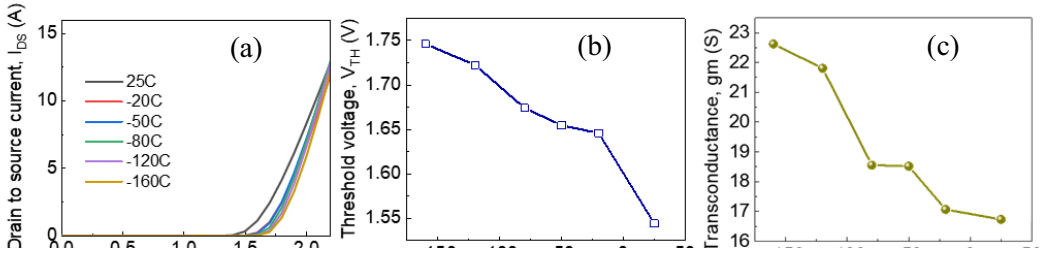

Figure 7. (a)transfer characteristics, (b) threshold voltage, (c) transconductance at different temperatures for a 600 V commercial GaN GIT device.

6. Cryogenic Temperature Scaling

The available compact models that take operating temperature as parameter are not adequate in the cryogenic regime. However, the effect of temperature on 2DEG is not very straightforward. The origin of 2DEG is not only from the polarization charge, but also from the AlGaN surface trap density that is dependent on the fabrication conditions. The location and level of the traps would have different effect on the 2DEG density. Different trap level would affect the effective Schottky barrier height thereby having different thermionic effect. Therefore, a simpler approach using curve fitting algorithm has been implemented. The proposed temperature scaling equations are listed in equations 8-10:

$$V_{th}(T_j) = V_{th}(T_{nom}) + TCVT1 \cdot (T_j - T_{nom}) + TCVT2 \cdot (T_j - T_{nom})^2 \quad (8)$$

$$K_p(T_j) = K_p(T_{nom})\left[TCB0 + TCB1\left(\frac{T_j}{T_{nom}}\right)^{BEXP}\right] \quad (9)$$

$$R_{drift}(T) = R_{drift}(25^0C) + (T - T_{nom})[R_{TC1} + R_{TC2}(T - T_{nom})]_{300} \quad (10)$$

Here, TCVT1, TCVT2, TCB0, TCB1, RTC1, RTC2, BEXP are the temperature dependent parameters for threshold voltage, transconductance and drift resistance respectively. Please note that Equation (10) has been rearranged according to Horner's rule [18] which is computationally favorable.

7. Parameter Extraction

The parameter extraction for room temperature I-V and C-V is detailed in [11]. For the temperature dependent parameter extraction, at first the isothermal measurements were taken for 25^0C down to -184^0C. After that, the model parameters were extracted for different temperatures by disabling the temperature scaling coefficients. After extracting the temperature dependent parameters, an empirical fitting function best suited for the behaviour was extracted.

8. Convergence Study

It is necessary to ensure that the device model shows robust convergence in simulating complex topologies. The load voltage waveform is demonstrated in Figure 8. An alternative phase disposition (APOD) PWM scheme has been selected to generate the 5-levels, namely $+2V_{dc}$, V_{dc}, 0, $-V_{dc}$, and $-2V_{dc}$, where V_{dc} is the dc bus voltage. As expected, the V_{out} output five voltage levels, which verifies that the inverter works properly [3]. It should be noted that the vendor's model fails to converge in this simulation.

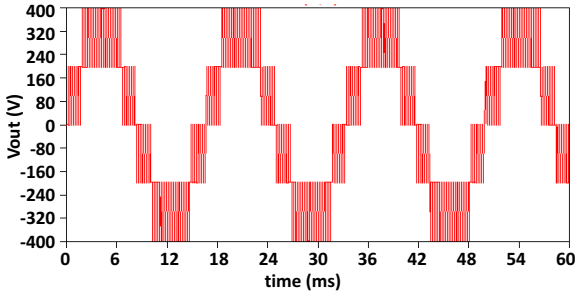

Figure 8. Output voltage waveforms for a 5-level CHB inverter.

9. Experimental Validation

A Double Pulse Test (DPT) for GaN GIT was performed on a commercial evaluation. The switching performance of the DUT can be assessed with the help of a DPT test. The measured and simulated I_{ds} switching waveforms are shown in Figure 9.

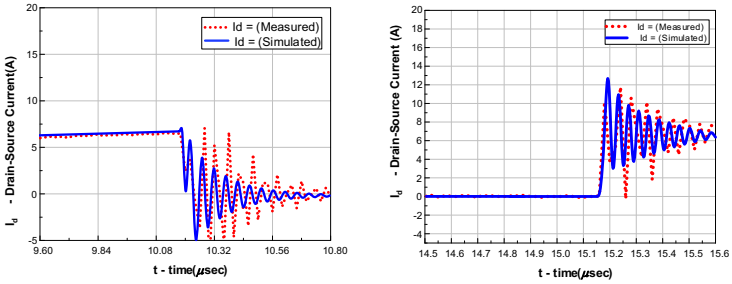

Figure 9. I_{ds} waveform for (a) turn off and (b) turn on transients.

10. Conclusion

This paper aims to implement a semi physics based GaN GIT model in LTspice with accurate static and dynamic behavior including cryogenic behavior modeling. It includes the conductivity modulation resulting from the hole injection. Furthermore, an additional complicated converter circuit, such as a 5-level Cascaded H-Bridge (CHB) multilevel inverter has been simulated to demonstrate the convergence robustness. This model will provide a means for designers to select the best devices for appropriate wide temperature range.

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